



PCB Protection: Choosing the Right Method

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With the continuing improvement of component packages in both weight and size, the need for an improved conformal coating increases for preventing contamination and moisture ingress. Reductions in overall component dimensions and pitch have increased the probability of dendritic growth and corrosion if an adequate conformal coating is not applied - and applied correctly. Where a conformal coating provides excellent protection for one component package, it does not always provide the same protection for another. A comprehensive test protocol including multiple types of component packages is needed to evaluate and select a conformal coating for your printed circuit board (PCB).

A test specimen should be used that replicates the hardware configuration of the PCB that is to be coated. Current test substrates available only contain a comb pattern for determining the presence of contaminants as indicated by a drop in surface insulation resistance (SIR). However, many of the substrates designed today include a mixture of surface mount components such as chip components, MELF components, SOIC's, TSOP's, QFP's, and BGA's of various dimensions and pitches. One test specimen designed by Soldering Technology International, Inc. (STI) incorporates a variety of daisy-chained components to test for dendritic growth and corrosion. The PCB contains two 0.5 mm pitch QFP's, two 0.5 mm pitch TSOP's, four 1.27 mm pitch PBGA's, and twelve 0805 chip resistors. The QFP and TSOP each contain a double-daisy chain for applying a voltage bias, determining insulation resistance, and monitoring for intermittent failures such as shorts and opens while the PBGA contains four perimeter row daisy chains. The manufacturing process employed when assembling the test specimen should be matched as closely as possible to that of the actual hardware.

The first step in the test protocol is ensure that proper manufacturing processes and handling do not introduce any ionic contaminants to the PCB. If a cleanliness level is not specified when procuring circuit boards, PCB's from a lot should randomly be ionograph tested for approved cleanliness levels. Results above the approved microgram NaCl/sq.in. level may require an additional cleaning step of bare circuit boards prior to assembly. An additional ionograph test should be conducted post-assembly before applying a conformal coating to ensure that ionic contaminants will not be trapped by the applied coating.

In order to evaluate the ability of a conformal coating to prevent moisture ingress, act as a barrier to surface contaminants, and provide surface insulation, standards have been developed for electrical and environmental screening. Several test methods are already available for determining the effectiveness of applied conformal coatings on a PCB. IPC, JEDEC, and Mil-Specs are available for electrical and environmental testing. STI prefers a combination of approved EIA/JEDEC and IPC standard test methods. IPC-TM-650 Method 2.6.3.4 outlines a testing procedure for determining moisture ingress and SIR values of conformal coatings. It also outlines a procedure for determining the susceptibility of the conformal coating to electrochemical migration

(ECMR) by placing a voltage bias on adjacent conductors. STI incorporates the procedure outlined in this IPC test method with the temperature range outlined in JESD22-A101-B, Steady State Temperature Humidity Bias Life Test. STI's modified test protocol follows the procedure below for determining the insulation resistance and level of moisture ingress of conformal coatings under accelerated temperature and humidity conditions.

STI Conformal Coating Evaluation Procedure:

Condition the specimen at 50°C with no added humidity for a period of 24 hours to completely dry the test assembly prior to electrical and environmental testing.

STI Conformal Coating Evaluation Procedure (Cont.)

2. Allow the specimen to cool prior to recording an initial insulation resistance measurement. Record the insulation resistance by applying 100 VDC to the test specimen as shown below. The minimum allowable resistance is 100 MΩ.

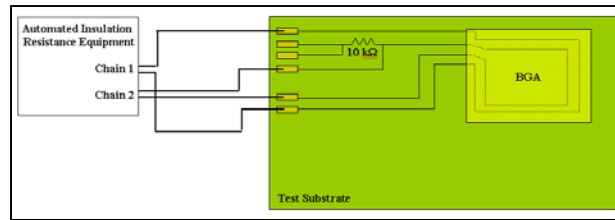


Figure 1. SIR testing configuration with STI test specimen.

3. Place specimen in a humidity/temperature cycle chamber and apply 10 VDC bias to alternating daisy chains. The presence of corrosion/dendritic growth shall be noted by a voltage drop across the 10 kΩ resistors placed in series with the grounded connections. An approximate 9 VDC drop will indicate a 1000Ω resistance dendritic growth/corrosion between adjacent rows.

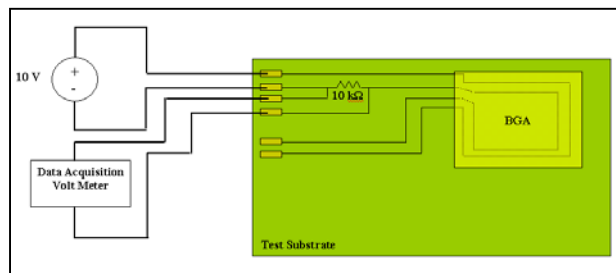


Figure 2. ECMR testing configuration with STI test specimen.

4. Expose test specimen to 10 cycles of temperature while maintaining 85%RH. Polarization voltage shall be maintained throughout the entire 10-cycle period. One cycle is as follows:
 - A. Start test at 25° C and raise the temperature to 85° C over a time span of 2 hours.
 - B. Maintain temperature at 85° C for 4 hours.

- C. Lower the temperature from 85° C to 25° C over a time span of 2 hours.
- D. Maintain temperature at 25° C for 4 hours.
- E. Complete sequence A-D a total of 4 times for completion of 1 cycle.

Note: There shall be no delay between cycles.

- 5. A data acquisition system shall monitor the voltage drop across each resistor to record any occurrences of this during humidity/temperature cycling. Voltage data shall be acquired every 60 seconds.
- 6. Every other thermal cycle (2, 4, 6, 8) the 10 VDC bias shall be disconnected and an insulation resistance test be conducted with the application of 100 VDC to the STI test specimen. Upon completion of the 10 thermal cycles, the test specimens shall be maintained at 25°C, 50% RH before the final insulation resistance test.

STI's proposed test protocol combines the strengths of both the IPC and the JEDEC standard test methods. The IPC test method provides validation of the conformal coating to act as a protective barrier to moisture and contamination under a cyclic thermal and humid environment, as well as promotes electromigration with the application of a 10 VDC bias on alternating daisy chains. In addition, the JEDEC test method promotes condensation due to the elevated temperature range of 85°C. The combined test protocol provides a more comprehensive evaluation of a conformal coating's ability to prevent electronic failures initiated by dendritic growth/corrosion. STI's designed test specimen and modified test protocol together offer a better screening method for choosing the proper conformal coating for a PCB.

To receive more information or to have STI perform this test for you, contact Casey Hatcher at 256-705-5511 or email at chatcher@solderingtech.com.